

CLAIMS

What is claimed is:

1 1. A method, comprising:
2 issuing an advanced load instruction with a first instance of a
3 first destination register;
4 decoding a test instruction with a second instance of said first
5 destination register where said second instance of said first destination
6 register is decoded as a first source register;
7 register renaming said first instance of said first destination
8 register and said first source register to a first physical register; and
9 validating results of said advanced load instruction using said
10 test instruction with said first physical register.

1 2. The method of claim 1, wherein said test instruction is a
2 load conditional instruction with said second instance of said first
3 destination register.

1 3. The method of claim 2, further comprising register
2 renaming said second instance of said first destination register to a
3 second physical register.

1 4. The method of claim 3, wherein said test instruction
2 operates to move contents of said first physical register to said second
3 physical register when said validation indicates said results are valid.

1 5. The method of claim 1, wherein said test instruction is a
2 speculation check instruction with said second instance of said first
3 destination register.

1 6. The method of claim 1, wherein said validating includes
2 searching a table for an entry with said first physical register.

1 7. A processor, comprising:
2 a decoder to decode a test instruction with a first instance of a
3 first destination register corresponding to a advanced load instruction
4 with a second instance of said first destination register wherein said
5 first instance is decoded as a first source register; and
6 a register renaming stage to rename said second instance of said
7 first destination register and said first source register to a first physical
8 register.

1 8. The processor of claim 7, wherein said test instruction is a
2 load conditional instruction.

1 9. The processor of claim 8, wherein said register renaming
2 stage to rename said first instance of said first destination register to a
3 second physical register.

1 10. The processor of claim 9, wherein said load conditional
2 instruction operates to move contents of said first physical register to
3 said second physical register when a validation circuit indicates that
4 results of said advanced load instruction are valid.

1 11. The processor of claim 10, wherein said validation circuit is
2 an advanced load address table.

1 12. The processor of claim 7, wherein said test instruction is a
2 speculation check instruction.

1 13. The processor of claim 12, wherein said speculation check
2 instruction is a no-operation when a validation circuit indicates that
3 results of said advanced load instruction are valid.

1 14. The processor of claim 13, wherein said validation circuit is
2 an advanced load address table.

1 15. A processor, comprising:
2 means for issuing an advanced load instruction with a first
3 instance of a first destination register;
4 means for decoding a test instruction with a second instance of
5 said first destination register where said second instance of said first
6 destination register is decoded as a first source register;
7 means for register renaming said first instance of said first
8 destination register and said first source register to a first physical
9 register; and
10 means for validating results of said advanced load instruction
11 using said test instruction with said first physical register.

1 16. The processor of claim 15, wherein said test instruction is a
2 load conditional instruction with said second instance of said first
3 destination register.

1 17. The processor of claim 16, further comprising means for
2 register renaming said second instance of said first destination register
3 to a second physical register.

1 18. The processor of claim 17, wherein said test instruction
2 operates to move contents of said first physical register to said second
3 physical register when said validation indicates said results are valid.

1 19. The processor of claim 15, wherein said test instruction is a
2 speculation check instruction with said second instance of said first
3 destination register.

1 20. The processor of claim 15, wherein said means for
2 validating includes a table searchable for an entry with said first
3 physical register.

1 21. A system, comprising:
2 a processor including a decoder to decode a test instruction with
3 a first instance of a first destination register corresponding to a
4 advanced load instruction with a second instance of said first
5 destination register wherein said first instance is decoded as a first
6 source register, and a register renaming stage to rename said second
7 instance of said first destination register and said first source register to
8 a first physical register;
9 an interface to couple said processor to input-output devices; and
10 an audio input-output circuit coupled to said interface and to
11 said processor.

1 22. The system of claim 21, wherein said test instruction is a
2 load conditional instruction.

1 23. The system of claim 22, wherein said register renaming
2 stage to rename said first instance of said first destination register to a
3 second physical register.

1 24. The system of claim 23, wherein said load conditional
2 instruction operates to move contents of said first physical register to
3 said second physical register when a validation circuit indicates that
4 results of said advanced load instruction are valid.

1 25. The system of claim 24, wherein said validation circuit is an
2 advanced load address table.

1 26. The system of claim 21, wherein said test instruction is a
2 speculation check instruction.

1 27. The system of claim 21, wherein said speculation check
2 instruction is a no-operation when a validation circuit indicates that
3 results of said advanced load instruction are valid.

1 28. The system of claim 27, wherein said validation circuit is an
2 advanced load address table.